

# ARTESYN DS1200HE

1200 Watts Distributed Power System



Advanced Energy's Artesyn DS1200 series is Artesyn Embedded Power' highest power, highest density bulk front end AC-DC power supply in the industry standard 1U x 2U form factor. It accepts a wide range 90–264 Vac input and provides a main 12 V output plus a 3.3 V or optional 5.5 V standby output. Rated at 1,100 watts, it has a high half-load efficiency of 91%. Housed in an industry standard 1U x 2U rack-mounting package, the power supply is designed for servers and similar space-constrained applications. This series comes in two airflow versions – dc-connector to ac-connector and vice versa.

#### **SPECIAL FEATURES**

- 1200 W output power
- High power
- 1U x 2U power supply
- High density design: 21.66 W/in<sup>3</sup>
- Active Power Factor Correction
- EN61000-3-2 Harmonic compliance
- Inrush current control
- 80plus Platinum efficiency
- N+1 or N+N redundant
- Hot plug operation
- N + 1 redundant
- Active current sharing
- Full Digital control
- PMBus compliant

- Input power reporting
- Compatible with Artesyn's Universal PMBus GUI
- Reverse airflow option
- Two-year warranty

#### COMPLIANCE

- Conducted/Radiated EMI Class B
- RoHS

#### SAFETY

- UL/cUL 60950 (UL Recognized)
- NEMKO+ CB Report EN60950
- CE Mark
- China CCC

### DATA SHEET

#### **Front-end Bulk Power**

#### **Total Output Power:**

180 to 264 Vac: 1200 W continuous 90 to 140 Vac: 1000 W/ 1200 W<sup>1</sup> continuous





## **ELECTRICAL SPECIFICATIONS**

Input	
Input voltage range	90 - 140 Vac: 1000 W/1200 W <sup>1</sup> 180 - 264 Vac: 1200 W
Frequency	47 Hz to 63 Hz
Efficiency	94.0% peak
Max input current	15 Arms
Inrush current	55 Apk at 240 Vac, cold start
Conducted EMI	Class B
Radiated EMI	Class B
Power factor	0.9 typical
ITHD	10%
Leakage current	1.4 mA
Hold-up time	12 ms

1 1000 W at forward air, 1200 W at reverse air. See power derating table

Ordering Information	
DS1200HE-3	12 V / 100 A, 3.3 Vsb / 6 A, standard airflow
DS1200HE-3-002	12 V / 100 A, 5.0 Vsb / 4 A, standard airflow
DS1200HE-3-003	12 V / 100 A, 3.3 Vsb / 6 A, reverse airflow
DS1200HE-3-004	12 V / 100 A, 5.0 Vsb / 4 A, reverse airflow

# **ELECTRICAL SPECIFICATIONS**

Output			
Main DC Output	MIN	NOM	MAX
Nominal setting	-0.50%	12	0.50%
Total output regulation range	11.4 V		12.6 V
Dynamic load regulation range	11.4 V		12.6 V
Output ripple			120 mVp-p
Output current	0 A4		100.0 A
Current sharing		Within ±5% of full load ratin	·
Capacitive loading	2,000 uF		40,000 uF
Start-up from AC to output			2000 ms
Output rise time	5 ms		50 ms



# ELECTRICAL SPECIFICATIONS (CONTINUED)

Standby DC Output (VSB)			
Output setpoint range	-1%	3.3 V (5.0 V)	1%
Total output regulation range	+5%		-5%
Dynamic load regulation range	+5%		-5%
Output ripple			50 mVp-p
Output current	0		6.0 A (4 A)
Current sharing		N/A	
Capacitive loading	0 uF		680 uF
Start-up from AC to output			1000 ms
Output rise time	2 ms		50 ms
Protections			
Protections			
Main Output			
Overcurrent protection <sup>2</sup>	120%		150%
Overvoltage protection <sup>1</sup>	13.5 V		15.0 V
Undervoltage protection	10.5 V		11.0 V
Overtemperature protection		Yes	
Fan fault protection		Yes	
Standby Output			
Overcurrent protection <sup>3</sup>			
Overvoltage protection <sup>3</sup>			

1 Latch mode

 $^2$  Autorecoverys if the overcurrent is less than 130% and last only for <1000 ms. Otherwise, latch mode

<sup>3</sup> Standby protection is auto-recovery
 <sup>4</sup> For output transient testing, the minimum load shall be at 10 A



# CONTROL AND STATUS SIGNALS

PSON_L			
	signal which enables/disables the main output. Pulling this signal L	OW will turn-on the main output.	
A 100pF deco	oupling capacitor is recommended at the system side.		1
		MIN	MAX
V <sub>IL</sub>	Input logic level LOW		0.8 V
V <sub>IH</sub>	Input logic level HIGH	2.0 V	5.0 V
SOURCE	Current that may be sourced by this pin		2 mA
SINK	Current that may be sunk by this pin at low state		0.5 mA
PSKILL_L			
First break/la	st mate active LOW signal which enables/disables the main outpu	t. This signal will have to be pulle	ed to ground at the system side with
220 ohm resis	stor. A 100 pF decoupling capacitor is also recommended.		
		MIN	MAX
V <sub>IL</sub>	Input logic level LOW		0.8 V
V <sub>IH</sub>	Input logic level HIGH	2.0 V	5.0 V
SOURCE	Current that may be sourced by this pin		2 mA
SINK	Current that may be sunk by this pin at low state		0.5 mA
VSENSE+, VS Output Signa	SENSE-, STBY_VSENSE+ ENSE-, and STBY_VSENSE+ lines are the remote sense lines for re als to indicate the presence of AC input to the power supply. A logic le		
VSENSE+, VSI Output Signa ACOK_L Signal used to the operating This is an ope	ENSE-, and STBY_VSENSE+ lines are the remote sense lines for re als	vel HIGH will indicate that the AG	C input to the power supply is within the power supply. It is recommended
VSENSE+, VSI Output Signa ACOK_L Signal used to the operating This is an ope	ENSE-, and STBY_VSENSE+ lines are the remote sense lines for re als o indicate the presence of AC input to the power supply. A logic le g range while a logic level LOW will indicate that AC has been lost. en collector/drain output. This pin is pulled high by a 1.0 kohm resi	vel HIGH will indicate that the AG	C input to the power supply is within the power supply. It is recommended
VSENSE+, VSI Output Signa ACOK_L Signal used to the operating This is an ope that this pin b	ENSE-, and STBY_VSENSE+ lines are the remote sense lines for re als o indicate the presence of AC input to the power supply. A logic le g range while a logic level LOW will indicate that AC has been lost. en collector/drain output. This pin is pulled high by a 1.0 kohm resi	vel HIGH will indicate that the AG istor connected to 3.3 V inside th by a 100 kohm resistor at the syst	C input to the power supply is within the power supply. It is recommended tem side.
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VSENSE+, VS Output Signa ACOK_L Signal used to the operating This is an ope that this pin b V <sub>IL</sub> V <sub>IL</sub> V <sub>IH</sub>	ENSE-, and STBY_VSENSE+ lines are the remote sense lines for re als to indicate the presence of AC input to the power supply. A logic le grange while a logic level LOW will indicate that AC has been lost. en collector/drain output. This pin is pulled high by a 1.0 kohm resi pe connected to a 100 pF decoupling capacitor and pulled down b Output logic level LOW Output logic level HIGH	vel HIGH will indicate that the AG istor connected to 3.3 V inside th by a 100 kohm resistor at the syst MIN	C input to the power supply is within the power supply. It is recommended tem side. MAX 0.6 V 5.0 V
VSENSE+, VSI Output Signa ACOK_L Signal used to the operating This is an ope	ENSE-, and STBY_VSENSE+ lines are the remote sense lines for re als to indicate the presence of AC input to the power supply. A logic lee g range while a logic level LOW will indicate that AC has been lost. en collector/drain output. This pin is pulled high by a 1.0 kohm resi- be connected to a 100 pF decoupling capacitor and pulled down be Output logic level LOW Output logic level LOW Output logic level HIGH Current that may be sourced by this pin Current that may be sunk by this pin at low state	vel HIGH will indicate that the AG istor connected to 3.3 V inside th by a 100 kohm resistor at the syst MIN	C input to the power supply is within the power supply. It is recommended tem side. MAX 0.6 V 5.0 V 3.3 mA
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## CONTROL AND STATUS SIGNALS (CONTINUED)

#### **Output Signals**

PS\_PRESENT

Signal used to indicate to the system that a power supply is inserted in the power bay. This pin is connected to ground via a 220 ohm resistor within the power supply

#### PS\_INTERRUPT

Active low signal used by the power supply to indicate to the system that a change in power supply status has occurred. This event can be triggered by faults such as OVP, OCP, OTP, and fan fault. This signal can be cleared by a CLEAR\_FAULT command. A 100pF decoupling capacitor is recommended.

		MIN	MAX
V <sub>IL</sub>	Output logic level LOW		0.8 V
V <sub>IH</sub>	Output logic level HIGH	2.0 V	5.0 V
I <sub>SOURCE</sub>	Current that may be sourced by this pin		4 mA
I <sub>SINK</sub>	Current that may be sunk by this pin at low state		4 mA
BUS Signals			
ISHARE			
Bus signal used l voltage inorder to	by the power supply for active current sharing. All power s o load share.	supplies configured in the system for n	+n sharing will refer to this bus
Voltage Range	The range of this signal for active sharing will be up to	8.0 V, which corresponds to the maxir	num output current.
		MIN	MAX
I <sub>SHARE</sub> Voltage	Voltage at 100% load, stand-alone unit	7.65	8.35
	Voltage at 50% load, stand-alone unit	3.65	4.35
	Voltage at 0% load, stand-alone unit	0	0.5
ISOURCE	Current that may be sourced by this pin		160 mA
SCL, SDA			
	ignals defined as per I <sup>2</sup> C requirements. It is recommended citor at the system side.	d that these pins be pulled-up to a 2.2	kohm resistor to 3.3 V and a 100 pF
		MIN	MAX
VL	Logic level LOW		0.8 V
V <sub>H</sub>	Logic level HIGH	2.0 V	5.0 V

Note: All signal noise levels are below 400 mVpk-pk from 0 - 100 MHz.



## **ELECTRICAL SPECIFICATIONS**

LED Indicators		
A single bi-color LED is used to indicate the power supply status.		
	Status LED	
No AC input to PSU	Off	
AC present, STBY ON, main output OFF	Blinking GREEN	
Main output ON	Solid GREEN	
Over-voltage/Under-voltage failure	Blinking AMBER	
Power supply failure (OVP, OTP, FAN FAULT)	Solid AMBER	

# I<sup>2</sup>C Addressing Table

PMBUS ADDRESSING		
Al	A0	Address
LOW	LOW	0 x B0
LOW	HIGH	0 x B2
HIGH	LOW	0 x B4
HIGH	HIGH	0 x B6

Firmware Reporting And Monitoring			
		MIN/	MAX
Output loading	5 to 20%	20% to 50%	50% to 100%
Input voltage		±5%	
Input current	±0.7 A fixed error	±5	%
Input power	±10 W at <125 W input	±5	%
Output voltage		±4%	
Output current	0.5 A fixed error	±5	%
Temperature	±5 degC on the operating range		
Fan speed	Actual ±250 RPM		

PMBus	YES
Remote ON/OFF	YES



# ELECTRICAL SPECIFICATIONS (CONTINUED)

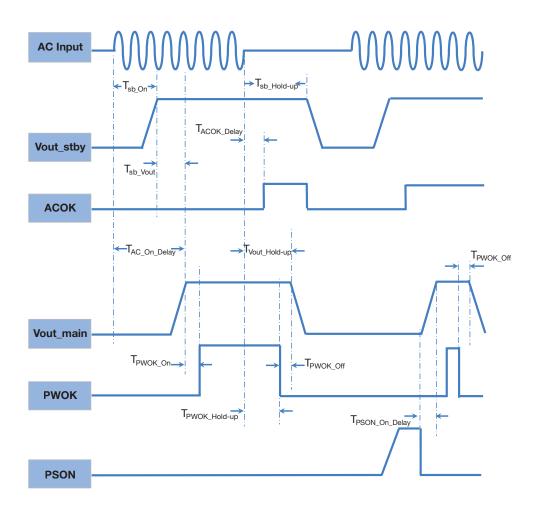
Timing Specification	ons			
	Description	Min	Max	Unit
T <sub>sb_On</sub>	Delay from AC being applied to standby output being within regulation		1700	ms
T <sub>AC_On_Delay</sub>	Delay from AC being applied to main output being within regulation		2000	ms
T <sub>PWOK_On</sub>	Delay from output voltages within regulation limits to PWOK asserted	100	1000	ms
T <sub>ACOK_Delay</sub>	Delay from loss of AC to assertion of ACOK	7	14	ms
T <sub>PWOK_Hold-up</sub>	Delay from loss of AC to deassertion of PWOK	11		ms
T <sub>Vout_Hold-up</sub>	Delay from loss of AC to main output being within regulation	12		ms
T <sub>sb_Hold-up</sub>	Delay from loss of AC to standby output being within regulation	400		ms
T <sub>PWOK_Off</sub>	Delay from deassertion of PWOK to output falling out of regulation	1		ms
T <sub>PSON_On_Delay</sub>	Delay from PSON assertion to output being within regulation		350	ms
T <sub>PWR_GOOD_Off</sub>	Delay from deassertion of PWOK to output falling out of regulation	1		ms
T <sub>PSON_On_Delay</sub>	Delay from PSON assertion to output being within regulation		350	ms

# ELECTRICAL SPECIFICATIONS

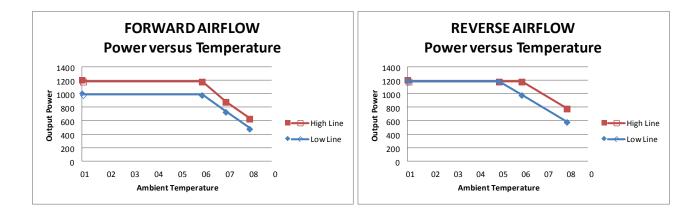
Operating temperature	-10 to 50 °C, can provide derated power up to 70 °C. See power derating curve
Operating altitude	Up to 10,000 feet
Operating relative humidity	10% to 90% non-condensing
Non-operating temperature	-40 to +85 °C
Non-operating relative humidity	10% to 95% non-condensing
Non-operating altitude	Up to 50,000 feet
Vibration and shock	Standard oprating/non-operating random shock and vibration
ROHS compliance	Yes
MTBF	200,000 hours using Bell Core TR-332, issue 6 specification, Method 1 Case 3 at 25 degC ambient at full load.
Operating life	Minimum of 5 years
Reliability	All electronic component derating analysis and capacitor life calculation is done as per Artesyn Network Power standards. The QAV report will be available upon request.

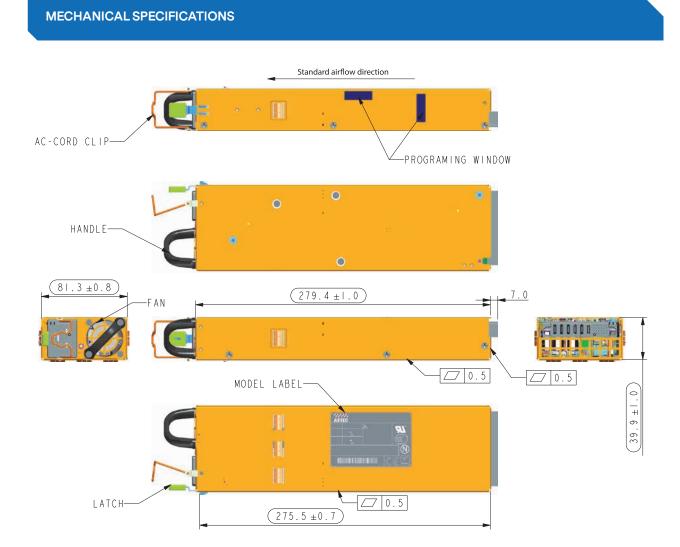


## **TIMING DIAGRAM**



#### **POWER DERATING CURVE**





## MECHANICAL SPECIFICATIONS

# DC Output Connector Pinout Assignment

Male connector as viewed from the rear of the supply:

D1	D2	D3	D4	D5	D6						
C1	C2	C3	C4	C5	C6	DD1	DDO	DDO	DD 4	DDC	DDO
B1	B2	B3	B4	B5	B6	PB1	PB2	PB3	PB4	PB5	PB6
A1	A2	A3	A4	A5	A6						

Power Supply Side 1. FCI Power Blade 51721 series 51721-10002406AA			
2. Molex Power Connector SD-87667 series 87667-7002			
Mating Connector (System Side)			
1. FCI Power Blade 51741-10002406CC Straight Pins			
2. FCI Power Blade 51761-10002406AALF Right Angle			
Any other approved equivalent			



# MECHANICAL SPECIFICATIONS (CONTINUED)

PinSignal NamePB1Main output returnPB2Main output returnPB3Main output returnPB4+ Main outputPB5+ Main outputPB6+ Main outputPB6+ Main outputPB6+ Main outputPB6+ Main outputPB6+ Main outputAllPS0N_LA2Main output remote sense return, VSENSE-A3SpareA4PS_PRESENTA5STAND-BY, 4YSBA6STAND-BY, 4YSBB1COK_H (AC Input Present)B2Main output remote sense, VSENSE+B3STAND-BY, ETURN, VSBB4STAND-BY, RETURN, VSBB4STAND-BYB5STAND-BY RETURNB6STAND-BY RETURNC1SCI (I'C Clock Signal)C2SCI (I'C Clock Signal)C3STAND-BY RETURNC4SpareC4SpareC4STAND-BY, 4YSBC6STAND-BY, 4YSBC6STAND-BY, 4YSBC6STAND-BY, 4YSBC6STAND-BY, 4YSBC7SCI (I'C Clock Signal)C8STAND-BY, 4YSBC9STAND-BY, 4YSB<		
P82Main output returnP83Main output returnP84Main outputP84Main outputP85Main outputP86Main outputP87Main outputP88Main output remote sense return, VSENSE-A1PSON_LA2Main output remote sense return, VSENSE-A3SpareA4PS_PRESENTA5STAND-BY, VSBA6STAND-BY RETURN, VSENSE+B1ACOK_H (AC Input Present)B2Main output remote sense, VSENSE+B3STAND-BY RETURN, VSENSE+B4PS_INHIBIT / PSKILL_LIB5STAND-BYB6STAND-BYC1SDA (I'C Data Signal)C2SCL (I'C Clock Signal)C3SPAREC6STAND-BY, NEBC6STAND-BY, RETURNC7SPAREC8SDA (I'C Data Signal)C9SPAREC9SPAREC9SPAREC6STAND-BY, AVSBC6STAND-BY, NEBC6STAND-BY, RETURNC6STAND-BY, RETURNC6AC (C Address BIT D Signal)C7AC (C Address BIT D Signal)C8STAND-BY, RETURNC9AC (C Address BIT Signal)C9SINDRERUPT (Alarm)C9SIND-BY, SINSER, VSENSE, STBYC9STAND-BY, SNBC9STAND-BY, SNBC9STAND-BY, SNBC9STAND-BY, SNBC9SINDRERUPT (Ala	Pin	Signal Name
PB3Main output returnPB4+ Main outputPB5+ Main outputPB6+ Main outputPB6+ Main outputPB6+ Main outputPB6> SON_LA1SonA1SareA3SareA4STAND-BY, AVSBA6STAND-BY, AVSBB1ACOK_H (AC Input Present)B2Sinterente sense, VSENSE-B3Sinterente sense, VSENSE-B4SYAND-BY RETURN, -VSBB4Sinterente sense, VSENSE-B5Sinterente sense, VSENSE-B6STAND-BYB7Sinterente sense, VSENSE-B6STAND-BYB7Sinterente sense, VSENSE-B6STAND-BYB7Sinterente sense, VSENSE-B6STAND-BYB7Sinterente sense, VSENSE-B6STAND-BYC1Sinterente sense, VSENSE-B6Sinterente sense, VSENSE-C2Sinterente sense, VSENSE-C3Sinterente sense, VSENSE-C4SenseC5Sinterente sense, VSENSE-C6Sinterente sense, VSENSE-D1ACI (Caderes BIT Signal)D2Aci (Caderes BIT Signal)D3Sinterente Sense)D4Sinterente Sense)D5Sinterente Sense)D5Sinterente Sense)D5Sinterente Sense)D5Sinterente Sense)D5Sinterente Sense)D5Sinterente Sense)<	РВ1	Main output return
PB4• Main outputPB5• Main outputPB6• Main outputA1PS0N_LA2Main output remote sense return, VSENSE-A3SpareA4PS_PRESENTA5STAND-BY, VSBA6STAND-BY, RETURN, VSBB1COCW_H (AC Input Present)B2Main output remote sense, VSENSE+B3STAND-BY RETURNB4STAND-BY RETURNB5STAND-BYB6STAND-BYC1SDA (IC Data Signal)C2SCI (IC Clock Signal)C3STAND-BY, HSIC4SPAREC5STAND-BY, SBC6STAND-BY, RETURND1OL (IC Clock Signal)C3STAND-BY, RETURNC4SpareC5STAND-BY, SBC6STAND-BY, RETURND1OL (IC Clock Signal)C6STAND-BY, SBC6STAND-BY, SBC6STAND-BY, SBC6STAND-BY, SBC6STAND-BY, SBC7A1 (IC Address BIT Signal)D2A1 (IC Address BIT Signal)D3STAND-BY, SSE, SENSYD5STAND-BY, SSE, SENSYD5STAND-BY, SSED5STAND-BY, SSED5STAND-BY, SSED5STAND-BY, SSE, SENSYD5STAND-BY, SSE, SENSYD5STAND-BY, SSE, SENSYD5STAND-BY, SSED5STAND-BY, SSED5STAND-BY, SSE	PB2	Main output return
PB5+ Main outputPB6+ Main outputA1PSON_LA2Main output remote sense return, VSENSE-A3SpareA4PS_PRESENTA5STAND-BY, +VSBA6STAND-BY, VSBB1ACOK_H (A Cinput Present)B2Main output remote sense, VSENSE+B3STAND-BYB4PS_INHIBIT/ PSKILLLIB5STAND-BYB6STAND-BY RETURNC1SOA (I'C Data Signal)C2SCA (I'C Clock Signal)C3STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, HTURNC1A0 (I'C Address BIT 0 Signal)C2STAND-BY, RETURNC6STAND-BY, RETURNC6STAND-BY, RETURNC6STAND-BY, RETURNC6STAND-BY, +VSBC6STAND-BY, RETURNC7A0 (I'C Address BIT 0 Signal)C8STAND-BY, RETURNC9A1 (I'C Address BIT 1 Signal)C9STAND-BY, RETURNC9STAND-BY, RETURNC9STAND-BY, RETURNC9STAND-BY, RETURNC9STAND-BY, RETURNC9STAND-BY, RETURNC9STAND-BY, RETURNC9STAND-BY, RETURNC9STAND-BY, RETURNC9STAND-B	РВЗ	Main output return
PB6+ Main outputA1PSON_LA2Main output remote sense return, VSENSE-A3SpareA4PS_PRESENTA5STAND-BY, +VSBA6STAND-BY, RETURN, -VSBB1ACOK_H (AC Input Present)B2Main output remote sense, VSENSE+B3ISHAREB4PS_INHIBIT / PSKILL_LIB5STAND-BY RETURNB6STAND-BY RETURNB7STAND-BY RETURNB6STAND-BY RETURNB7SCOK_H (AC Input Present)B6STAND-BY RETURNB7STAND-BY RETURNB6STAND-BY RETURNC1STAND-BY RETURNC2SCOK_H (CC Input Present)C3SCU (C'C Cock Signal)C4SpareC5STAND-BY RETURNC6STAND-BY RETURND1AC (I'C Address BIT A Signal)D2A(I'C Address BIT I Signal)D3STAND-BY RETURND4STAND-BY RETURND5STAND-BY RETURN	РВ4	+ Main output
A1PSN_LA2Main output remote sense return, VSENSE-A3SpareA4PS_PRESENTA5STAND-BY, 4VSBA6STAND-BY RETURN, -VSBB1ACOK_H (AC Input Present)B2Main output remote sense, VSENSE+B3STAND-BYB4PS_INHIBIT / PSKILL_LIB5STAND-BY RETURNB6STAND-BY RETURNB7STAND-BYB6STAND-BY RETURNC1SCA (I <sup>6</sup> C Clock Signal)C2SCA (I <sup>6</sup> C Clock Signal)C3STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, HURND1AQ (I <sup>6</sup> C Address BIT 0 Signal)D2A1 (I <sup>6</sup> C Address BIT 1 Signal)D3SP_INTERRUPT (Alarm)D4STAND-BY, HYSBD5STAND-BY, +VSB	PB5	+ Main output
A2Main output remote sense return, VSENSE-A3SpareA4PS_PRESENTA5STAND-BY, +VSBA6STAND-BY, PKTURN, -VSBB1ACOK_H (AC Input Present)B2Main output remote sense, VSENSE+B3STAND-BYB4STAND-BYB5STAND-BYB6STAND-BYC1STAND-BYC2SCL (°C Clock Signal)C3STAND-BY, +VSBC4SpareC5STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC6STAND-BY, +VSBC7AC (°C Clock SIgnal)C7AC (°C Address BIT 0 Signal)C8STAND-BY, RETURNC9SINTERRUPT (Alarm)C9SINTERRUPT (Alarm)C9SINTERRUPT (Alarm)C9SINTERRUPT (Alarm)C9SIND-BY, +VSBC9SIND-BY, +VSBC9 <t< td=""><td>PB6</td><td>+ Main output</td></t<>	PB6	+ Main output
A3SpareA4PS_PRESENTA5STAND-BY, 4/SBA6STAND-BY RETURN, -VSBB1ACOK_H (AC Input Present)B2Main output remote sense, VSENSE+B3ISHAREB4PS_INHIBIT / PSKILL_LIB5STAND-BY RETURNB6STAND-BY RETURNC1SDA (if C Data Signal)C2SCL (if C Clock Signal)C3STAND-BY, HSBC4STAND-BY, HSBC5STAND-BY, HSBC6STAND-BY, HSBC7STAND-BY, HSBC6STAND-BY, HSBC7STAND-BY, HSBC6STAND-BY, HSBC7STAND-BY, HSBC6STAND-BY, HSBC7AO (if C Address BIT 0 Signal)C9AI (if C Address BIT 1 Signal)C9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSB, SENSE, SENSE_STBYC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSB, SENSE, SENSE_STBYC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9STAND-BY, HSBC9ST	A1	PSON_L
A4         PS_PRESENT           A5         STAND-BY, +VSB           A6         STAND-BY RETURN, -VSB           B1         ACOK_H (AC Input Present)           B2         Main output remote sense, VSENSE+           B3         ISHARE           B4         PS_INHBIT / PSKILL_LI           B5         STAND-BY RETURN           B6         STAND-BY RETURN           C1         STAND-BY RETURN           C2         STAND-BY RETURN           C3         SCAL( <sup>1</sup> C Clock Signal)           C4         Spare           C5         STAND-BY RETURN           C6         STAND-BY RETURN           C6         SCAL( <sup>1</sup> C Clock Signal)           C7         SCALC           C6         STAND-BY, +VSB           C6         STAND-BY, HETURN           C6         STAND-BY, HETURN           C1         AC ( <sup>1</sup> C Address BIT O Signal)           C1         AC ( <sup>1</sup> C Address BIT O Signal)           C2         AL ( <sup>1</sup> C Address BIT Signal)           C3         AL ( <sup>1</sup> C Address BIT Signal)           C4         SIND-BY, FUTF (Alarm)           C5         SIND-BY, FUTS SINSE, SISTBY           C4         SIND-BY, FUTS SINSE, SISTBY	A2	Main output remote sense return, VSENSE-
A5         STAND-BY, +VSB           A6         STAND-BY RETURN, -VSB           B1         ACOK_H (AC Input Present)           B2         Main output remote sense, VSENSE+           B3         ISHARE           B4         PS_INHIBIT / PSKILL_LI           B5         STAND-BY RETURN           B6         STAND-BY           B6         STAND-BY           B7         STAND-BY	A3	Spare
A6STAND-BY RETURN, -VSBB1ACOK_H (AC Input Present)B2Main output remote sense, VSENSE+B3ISHAREB4PS_INHIBIT / PSKILL_LIB5STAND-BYB6STAND-BY RETURNC1SDA (I°C Data Signal)C2SCL (I°C Clock Signal)C3POWER GOOD/ PWOK_HC4SpareC5STAND-BY RETURND1AO (I°C Address BIT 0 Signal)C5STAND-BY RETURND1AO (I°C Address BIT 0 Signal)D2AI (I°C Address BIT 1 Signal)D3STAND-BY RETURND4STAND-BY RETURND4STAND-BY RETURND5STAND-BY RETURND6STAND-BY RETURND1AI (I°C Address BIT 0 Signal)D2STAND-BY RETURND4STAND-BY RETURND5STAND-BY RETURND5STAND-BY RETURND6STAND-BY RETURND7STAND-BY RETURND8STAND-BY RETURND9STAND-BY RETURND9STAND-BY RETURND1STAND-BY RETURND2STAND-BY RETURND3STAND-BY RETURND4STAND-BY RETURND5STAND-BY RETURND6STAND-BY RETURND7STAND-BY RETURND8STAND-BY RETURND9STAND-BY RETURND9STAND-BY RETURND9STAND-BY RETURND9STAND-BY RETURND9STAND-BY RETURND9	A4	PS_PRESENT
B1ACOK_H (AC Input Present)B2Main output remote sense, VSENSE+B3ISHAREB4PS_INHIBIT / PSKILL_LIB5STAND-BYB6STAND-BYC1SDA (I <sup>c</sup> Data Signal)C2SCL (I <sup>c</sup> Clock Signal)C3POWER GOOD/ PWOK_HC4SpareC5STAND-BY RETURND1A(I <sup>c</sup> Cadress BIT O Signal)D2A(I <sup>c</sup> Cadress BIT O Signal)D3PS_INTERRUPT (Alarm)D4SpinterRUPT (Alarm)D4STAND-BY RETURND5SIND-BY, VSBD6STAND-BY RETURND1A(I <sup>c</sup> CAddress BIT Signal)D2SINTERRUPT (Alarm)D4STAND-BY RETURND4SIND-BY, VSBD5SIND-BY, VSB	A5	STAND-BY, +VSB
B2     Main output remote sense, VSENSE+       B3     ISHARE       B4     PS_INHIBIT / PSKILL_LI       B5     STAND-BY       B6     STAND-BY       B6     STAND-BY RETURN       C1     SDA (r <sup>2</sup> C Data Signal)       C2     SCL (r <sup>2</sup> C Clock Signal)       C3     POWER GOOD/ PWOK_H       C4     STAND-BY RETURN       C6     STAND-BY, +VSB       C6     STAND-BY, et URN       D1     A0 (r <sup>2</sup> C Address BIT 0 Signal)       D2     A1 (r <sup>2</sup> C Address BIT 1 Signal)       D3     PS_INTERRUPT (Alarm)       D4     STAND-BY RMT SENSE, VSENSE_STBY       D5     STAND-BY, +VSB	A6	STAND-BY RETURN, -VSB
B3ISHAREB4PS_INHIBIT / PSKILL_LIB5STAND-BYB6STAND-BYB6STAND-BY RETURNC1SDA (i <sup>c</sup> Data Signal)C2SCL (i <sup>c</sup> Clock Signal)C3POWER GOOD/ PWOK_HC4SpareC5STAND-BY RETURND1Al (i <sup>c</sup> Datas BIT D Signal)D2Al (i <sup>c</sup> Caddress BIT D Signal)D3PS_INTERRUPT (Alarm)D4STAND-BY RETURND4SIND-BY RETURND5STAND-BY RETURND5STAND-BY RETURND6SIND-BY RETURND3SIND-BY RETURND4SINTERRUPT (Alarm)D4SIAND-BY RETURND4SIAND-BY RETURND4SIAND-BY RETURND5SIAND-BY RETURND4SIAND-BY RETURND5SIAND-BY RETURND6SIAND-BY RETURND6SIAND-BY RETURND7SIAND-BY RETURND8SIAND-BY RETURND9SIAND-BY RETU	B1	ACOK_H (AC Input Present)
B4PS_INHIBIT / PSKILL_LIB4PS_INHIBIT / PSKILL_LIB5STAND-BYB6STAND-BY RETURNC1SDA (r <sup>2</sup> C Data Signal)C2SCL (r <sup>2</sup> C Clock Signal)C3POWER GOOD/ PWOK_HC4SpareC5STAND-BY, +VSBC6STAND-BY RETURND1A0 (r <sup>2</sup> C Address BIT 0 Signal)D2S1 (r <sup>2</sup> C Address BIT 1 Signal)D3PS_INTERRUPT (Alarm)D4STAND-BY, +VSBD5STAND-BY, HYSBD4STAND-BY, HYSBD4STAND-BY, HYSBD5STAND-BY, HYSBD4STAND-BY, HYSBD5STAND-BY, HYSBD5STAND-BY, HYSBD6STAND-BY, HYSBD7STAND-BY, HYSBD4STAND-BY, HYSBD5STAND-BY, HYSBD5STAND-BY, HYSBD6STAND-BY, HYSBD7STAND-BY, HYSB <td>B2</td> <td>Main output remote sense, VSENSE+</td>	B2	Main output remote sense, VSENSE+
B5STAND-BYB6STAND-BY RETURNC1SDA (I <sup>2</sup> Data Signal)C2SCL (I <sup>2</sup> C Clock Signal)C3POWER GOOD/ PWOK_HC4SpareC5STAND-BY, +VSBC6STAND-BY RETURND1A0 (I <sup>2</sup> C Address BIT 0 Signal)D2A1 (I <sup>2</sup> C Address BIT 1 Signal)D3PS_INTERRUPT (Alarm)D4STAND-BY, +VSBD5STAND-BY, +VSBD4STAND-BY, +VSBD5STAND-BY, +VSBD6STAND-BY, +VSBD7STAND-BY, +VSBD4STAND-BY, +VSBD5STAND-BY, +VSB	B3	ISHARE
B6STAND-BY RETURNC1SDA (i <sup>2</sup> C Data Signal)C2SCL (i <sup>2</sup> C Clock Signal)C3POWER GOOD/ PWOK_HC4SpareC5STAND-BY, +VSBC6STAND-BY, RETURND1A0 (i <sup>2</sup> C Address BIT 0 Signal)D2A1 (i <sup>2</sup> C Address BIT 1 Signal)D3STAND-BY RETURY (Alarm)D4STAND-BY RMY SENSE, VSENSE_STBYD5STAND-BY, +VSB	B4	PS_INHIBIT / PSKILL_LI
C1       SDA (l <sup>2</sup> C Data Signal)         C2       SCL (l <sup>2</sup> C Clock Signal)         C3       POWER GOOD/ PWOK_H         C4       Spare         C5       STAND-BY, +VSB         C6       STAND-BY, RETURN         D1       A0 (l <sup>2</sup> C Address BIT 0 Signal)         D2       A1 (l <sup>2</sup> C Address BIT 1 Signal)         D3       STAND-BY, FWSB         D4       STAND-BY, RMT SENSE, VSENSE_STBY         D5       STAND-BY, +VSB	B5	STAND-BY
C2SCL (i <sup>2</sup> C Clock Signal)C3POWER GOOD/ PWOK_HC4SpareC5STAND-BY, +VSBC6STAND-BY RETURND1A0 (i <sup>2</sup> C Address BIT 0 Signal)D2A1 (i <sup>2</sup> C Address BIT 1 Signal)D3PS_INTERRUPT (Alarm)D4STAND-BY, +VSBD5STAND-BY, +VSB	B6	STAND-BY RETURN
C3POWER GOOD/ PWOK_HC4SpareC5STAND-BY, +VSBC6STAND-BY RETURND1A0 (i²C Address BIT 0 Signal)D2A1 (i²C Address BIT 1 Signal)D3PS_INTERRUPT (Alarm)D4STAND-BY RMT SENSE, VSENSE_STBYD5STAND-BY, +VSB	C1	SDA (l <sup>2</sup> C Data Signal)
C4SpareC5STAND-BY, +VSBC6STAND-BY RETURND1A0 (1 <sup>2</sup> C Address BIT 0 Signal)D2A1 (1 <sup>2</sup> C Address BIT 1 Signal)D3PS_INTERRUPT (Alarm)D4STAND-BY RETNENSE_STBYD5STAND-BY, +VSB	C2	SCL (l <sup>2</sup> C Clock Signal)
C5STAND-BY, +VSBC6STAND-BY RETURND1A0 (i²C Address BIT 0 Signal)D2A1 (i²C Address BIT 1 Signal)D3PS_INTERRUPT (Alarm)D4STAND-BY RMT SENSE, VSENSE_STBYD5STAND-BY, +VSB	C3	POWER GOOD/ PWOK_H
C6     STAND-BY RETURN       D1     A0 (l <sup>2</sup> C Address BIT 0 Signal)       D2     A1 (l <sup>2</sup> C Address BIT 1 Signal)       D3     PS_INTERRUPT (Alarm)       D4     STAND-BY RMT SENSE, VSENSE_STBY       D5     STAND-BY, +VSB	C4	Spare
D1     A0 (l <sup>2</sup> C Address BIT 0 Signal)       D2     A1 (l <sup>2</sup> C Address BIT 1 Signal)       D3     PS_INTERRUPT (Alarm)       D4     STAND-BY RMT SENSE, VSENSE_STBY       D5     STAND-BY, +VSB	C5	STAND-BY, +VSB
D2     A1 (l <sup>2</sup> C Address BIT 1 Signal)       D3     PS_INTERRUPT (Alarm)       D4     STAND-BY RMT SENSE, VSENSE_STBY       D5     STAND-BY, +VSB	C6	STAND-BY RETURN
D3     PS_INTERRUPT (Alarm)       D4     STAND-BY RMT SENSE, VSENSE_STBY       D5     STAND-BY, +VSB	D1	A0 (l <sup>2</sup> C Address BIT 0 Signal)
D4     STAND-BY RMT SENSE, VSENSE_STBY       D5     STAND-BY, +VSB	D2	A1 (l <sup>2</sup> C Address BIT 1 Signal)
D5 STAND-BY, +VSB	D3	PS_INTERRUPT (Alarm)
	D4	STAND-BY RMT SENSE, VSENSE_STBY
D6 STAND-BY RETURN, -VSB	D5	STAND-BY, +VSB
	D6	STAND-BY RETURN, -VSB



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