

**iVS Series** 

**Electrical Interface** 



# **Testing Result Summary\***

This Technical Reference Note describes how to use the power and signals available in iVS Case and modules. iVS supported PMBus commands and it's limitation is not covered in this application note.



Page 1

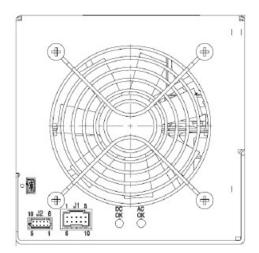


iVS Electrical Interface Page 2

#### **ELECTRICAL INTERFACE to iVS Case** 1.

The iVS cases (iVS1, iVS3, iVS6 and iVS8) has two signal connectors located in the front panel, J1 – PFC Input Connector and J2 – I2C Bus Output Connector, and two LEDs which serve as visual status indicators.

#### **iVS Front Panel**



A In *Pir* 1

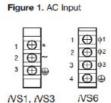
2

3

4

-----

#### **Pin Connectors**



NS1, NS3





phone i	 	

10 28 EI. . -. . . . .

Mates with Landwin 2050S1000 Housing 2053T011V Pin or

JST PHDR-10VS Housing JST SPHD-002T-P0.5 (28-24) JST SPHD-001T-P0.5 (26-22)

Connector Kit Part No .: 70-841-023

C put	Single Phase	3 Phase
n	Function	
	AC neutral	Line 1
	AC line (hot)	Line 2
	Chassis (earth) ground	Line 3
	Not used	Chassis (earth) ground

#### Figure 2. Connector J1



Mates with Molex 90142-0010 Housing 90119-2110 Pin

Connector Kit Part No .: 70-841-004

	lnput Connector htrol & signals)
Pin	Function
1	Input AC OK - "emitter"
2	Input AC OK - "collector"
3	Global DC OK - "emitter"
4	Global DC OK - "collector"
5	Spare
6	Global inhibit/optional enable logic "0"
7	Global inhibit/optional enable logic "1"
8	Global inhibit/optional enable return
9	+5 VSB housekeeping
10	+5 VSB housekeeping return

Pin	Function		
1	No connection		
2	No connection		
3	No connection		
4	Serial clock signal (SCL)		
5	Serial data signal (SDA)		
6	Address bit 0 (A0)		
7	Address bit 1 (A1)		
8	Address bit 2 (A2)		
9	Secondary return (GND)		
10	5 VCC external bus (5 VCC bus)		

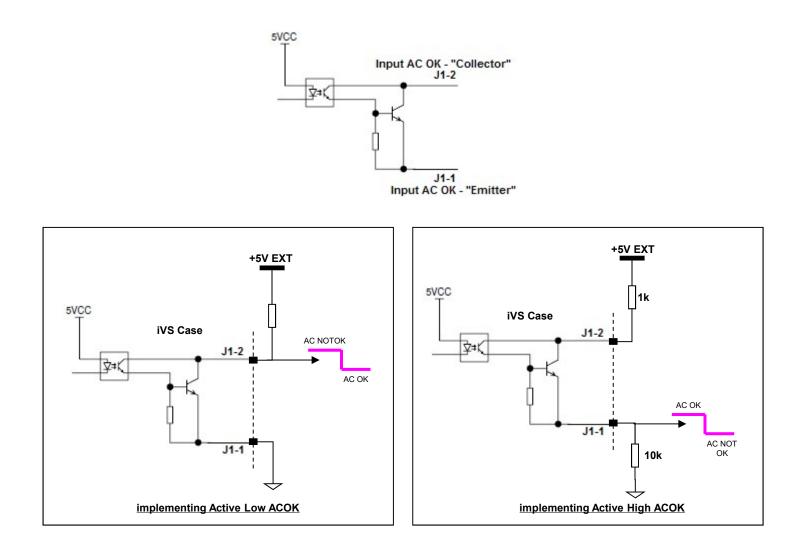


# **1.1** Pin Description of iVS case J1 – PFC Input connector.

## 1.1.1 INPUT ACOK SIGNAL (ACOK\_C/ACOK\_E) - Pins 1, 2

Input ACOK – "Collector" and Input ACOK – "Emitter" are output of an uncommitted bipolar junction transistor. The transistor shall turn ON when the Input Mains level is Good >85Vac, it shall turn OFF when input voltage is <85Vac. Sink Current: 50mA max, 5ms minimum warning time.

A green LED is provided in the iVS Case as visual indicator of the status of ACOK signal.

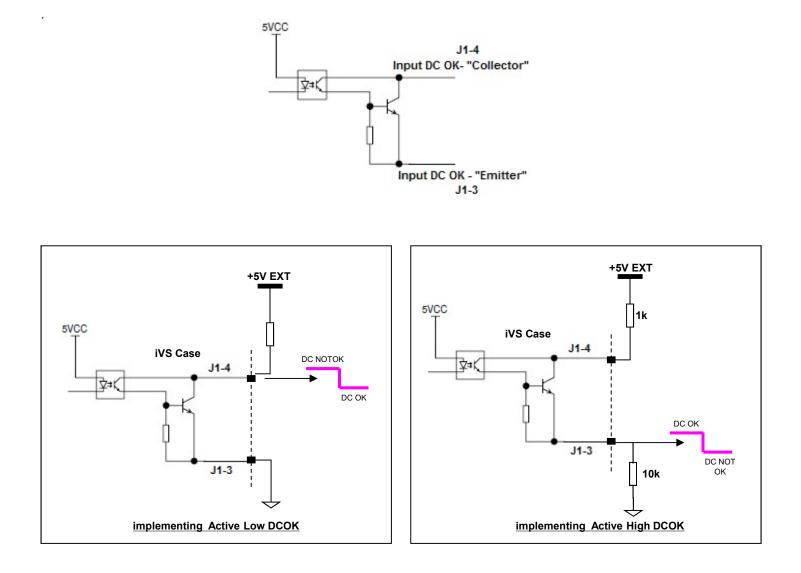




#### 1.1.2 GLOBAL DCOK SIGNAL (DCOK\_C/DCOK\_E) - Pins 3, 4

Global DCOK – "Collector" and Global DCOK – "Emitter" are output signal of uncommitted bipolar junction transistor. The transistor shall turn ON when the DC output of ALL modules are in good regulation, otherwise it shall turn OFF. A green LED is provided as a visual indicator of the DCOK status. Sink Current: 50mA max.

Page 4





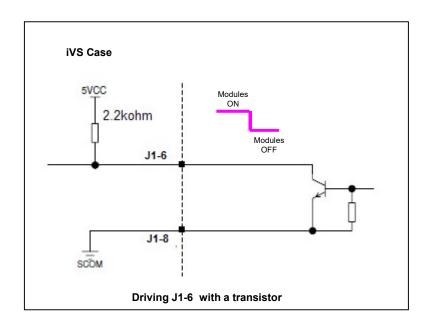
#### 1.1.3 GLOBAL INHIBIT/OPTIONAL ENABLE LOGIC "0" (DEFAULT) - Pin 6

This signal is a TTL input to a microcontroller inside the iVS case, an internal 2.2kohm resistor is connected between this pin and internal 5V supply to make the signal initially HIGH.

Enable Logic "0" (DEFAULT setting), active High is the default Logic when Global Enable Option is NOT selected.

When pin is left open or pull HIGH (2V - 5V), the modules are ON and can be disable/enable by PMBus OPERATION command. The Modules set to Module Option Code 1 'Module Enable mode' will remain OFF until enable by its Module Inhibit Pin.

When the pin is pull LOW (<0.8V) the modules will turn OFF, the PMBus OPERATION COMMAND alone cannot enable the modules.

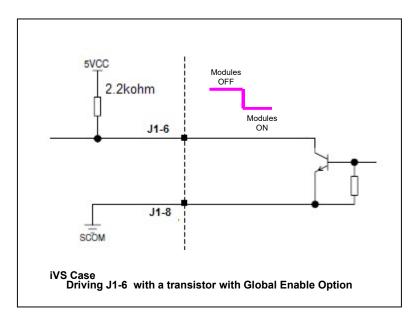




The logic of the signal is reverse when Case Option Code 3 - 'Global Enable option' is selected'.

When the pin is left open or pull HIGH (2V - 5V), all the Modules are OFF, the PMBus OPERATION COMMAND alone cannot enable the modules.

When pin is pull LOW (<0.8V), the Modules are ON and can be disable/enable by PMBus OPERATION COMMAND. The Modules set to Module Option Code 1 'Module Enable mode' will remain OFF enable by its Module Inhibit pin.





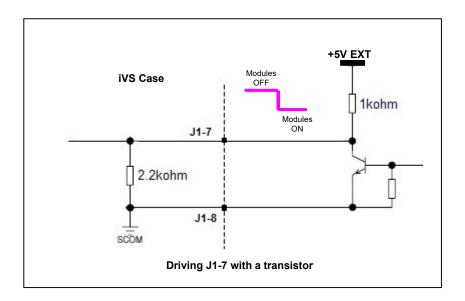
#### 1.1.4 GLOBAL INHIBIT/OPTIONAL ENABLE LOGIC "1" (DEFAULT) - Pin 7

This pin is a TTL input to a microcontroller inside the iVS case, an internal 2.2kohm resistor is connected between this pin and ground to make the signal initially LOW.

Logic "1" (Default), active LOW is the <u>default Logic when 'Global Enable Option' is NOT selected</u>. Upon application of correct AC input all the modules are ON except the modules set to Module Option code 1 'Module Enable mode'.

When pin is left open or pull LOW (<0.8V), the modules are ON and can be disable/enable by PMBus OPERATION COMMAND. The Modules set to Module Option Code 1 'Module Enable mode' will remain OFF until enable by its Module Inhibit pin.

When pin is pull HIGH (>2V- 5V), the installed modules will turn OFF, the PMBus OPERATION Command alone cannot enable the modules. The 5V standby output can be used as external supply to drive Pin 7.





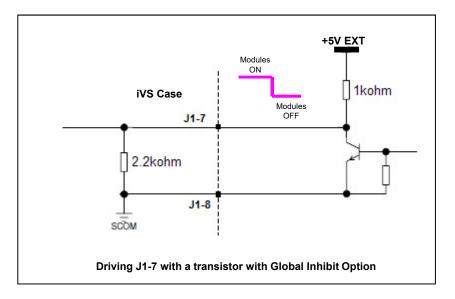
Page 8

The logic of the signal is reverse when Case Option Code3 - 'Global Enable option' is selected.

When pin is left open or pull LOW (<0.8V) all the Modules are OFF, the PMBus OPERATION Command alone cannot enable the modules.

When pin is pull HIGH (>2V- 5V), the Modules will turn ON and can be disable/enable by PMBus OPERATION COMMAND. The modules set to Module Option Code 1 'Module Enable mode' will remain OFF until enable by its Module Inhibit pin. The 5V standby output can be used to drive this pin.

Note: Pin 6 and Pin 7 are independent signals, both signals must assume the correct logic levels to turn ON the modules.





#### 1.1.5 GLOBAL INHIBIT/OPTIONAL ENABLE RETURN - Pin 8

Ground reference for Global Enable/Optional Enable. This pin is electrically connected to Pin 10 - +5Vsb Housekeeping Return.

#### 1.1.6 +5VSB HOUSEKEEPING – Pin 9

+5Vsb Housekeeping is the standby output of the power supply rated 5V/1A. This output is available every time the input AC voltage to the power supply is within 85Vac - 264Vac. This output is not affected by Global Inhibit function.

#### 1.1.7 +5VSB HOUSEKEEPING RETURN - Pin 10

The ground reference of +5Vsb housekeeping, this ground is not connected to the chassis of the power supply.

## 1.2 Pin Description of iVS case J2 – I2C Bus Output connector.

#### 1.2.1 5VCC BUS - Pin 10

This pin is an input to the iVS Case, applying 5V to this signal will provide external power to the I2C devices - EEPROM and Microcontroller. The pin can be used to enable the I2C communication using external power supply and allow reading of manufacturing from a non-working PSU without powering the supply. Do not supply voltage >5.5V to prevent damaging the I2C devices.

#### 1.2.2 SECONDARY RETURN (GND) - Pin 9

Ground Reference for the signals of J2 connector. This pin is electrical connected to Pin 10 = +5Vsb Housekeeping Return of J1 connector.

#### 1.2.3 SERIAL DATA SIGNAL (SDA) and SERIAL DATA CLOCK (SCL) -Pins 4, 5

These are pins for I2C communication and must be pulled-up in the system by 1K ohm resistor to 5V Housekeeping; a current source pull-up can also be used. If multiple units are used inside a system, the 5V Housekeeping of each unit must be connected in parallel in the system, otherwise, the SCL and SDA bus will be pulled low by the unit without AC power.

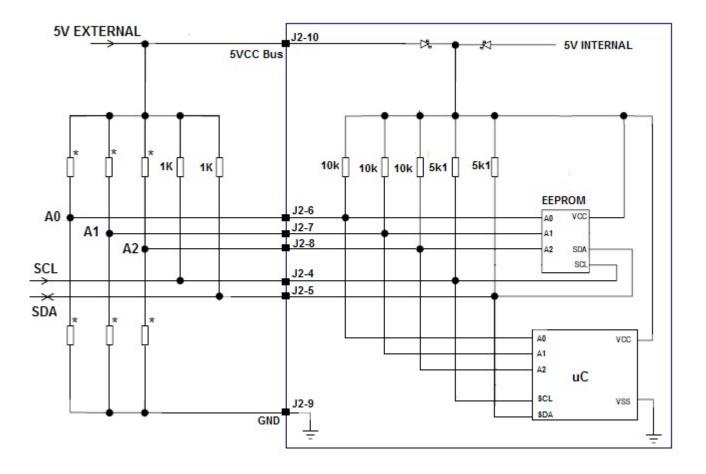


#### 1.2.4 ADDRESS PINS A0, A1, AND A2 - Pins 6, 7, 8

Multiple configured iVS power supplies can be used in a single system, the power supplies can have parallel outputs or providing multiple outputs. The iVS CASE has three address pins allowing the system to assign different addresses to multiple PSUs used within the system. The I2C devices inside the iVS-CASE are EEPROM to store FRU data and microcontroller for PMBus. The table below listed all the possible addresses of the two I2C devices inside the PSU. Pull the address pin to Secondary Return (COM) to set the address to "0" or High (or open) to set it the address to "1".

<b>A0</b>	A1	A2	EEPROM	CASE MICROCONTROLLER
0	0	0	0xA0	0x30
0	0	1	0xA2	0x32
0	1	0	0xA4	0x34
0	1	1	0xA6	0x36
1	0	0	0xA8	0x38
1	0	1	0xAA	0x3A
1	1	0	0xAC	0x3C
1	1	1	0xAE*	0x3E*

This is the default address when A0,A1,A2 are left open.



I2C connection diagram. The Address A0, A1, A2 can be either pull high to Vcc or pull down to COM.



### 1.3 LED Behavior

There are two green LEDs in iVS front panel that serves as visual indication of the power supply status. The table below describes the symptom for each LED behavior.

CONDITION	DCOK LED	ACOK LED
AC Present, Outputs Inhibited (Case Global Inhibit)	BLINKING	ON
AC Present, Outputs Inhibited (Module Isolated Inhibit)	OFF	ON
AC Present, Outputs Enabled	ON	ON
Output OCP/OVP/Fan Fault	OFF	ON
AC Not Present	OFF	OFF



# 2. ELECTRICAL INTERFACE TO THE OUTPUT MODULES

# 2.1 Pin Description of Module J1 – Control Connector.

144 W

The following pin descriptions are applicable to single output and dual output modules.

Note: The pin numbering of Module J1 connector was made compatible with previous generation MP series, it may differ from the numbering in the vendor connector drawing (e.g. Molex).



210 W



360 W



750 W



1500 W

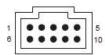
# **iMP Modules**

## **DC-DC Converter Output Modules**

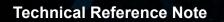
Pin No.	Function		
1	+ Remote Sense	single or dual o/p main	
2	Remote Margin / V. Program	single o/p	
3	Margin High	single o/p	
4	- Remote Sense / Margin Low	single or dual o/p main	
5	Spare		
6	Module, Isolated Inhibit	single or dual o/p	
7	Module Inhibit Return	single or dual o/p	
8	Current Share (SWP)	single or dual o/p main	
9	+ Remote Sense V2	dual o/p, single is spare	
10	- Remote Sense V2	dual o/p, single is spare	

\* Note: All IMP modules have a green DCOK LED. (except for 36 W module)

#### Figure 4. Connector J1



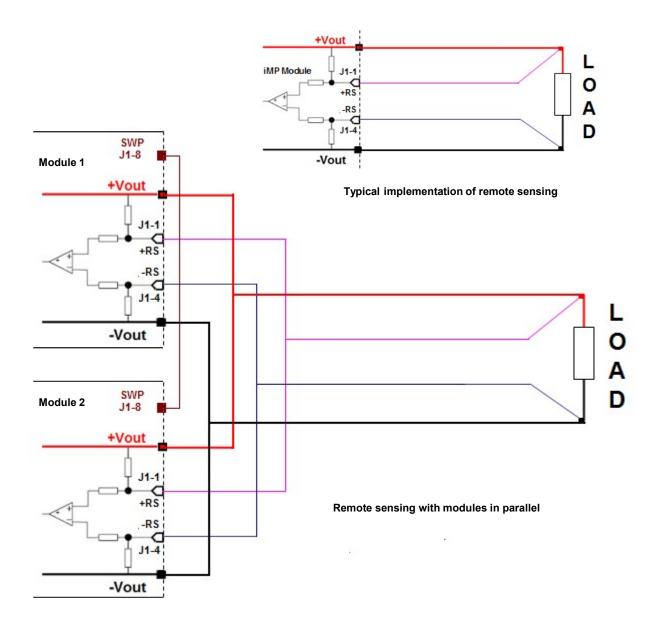
Mates with Molex 90142-0010 Housing 90119-2110 Pin



#### 2.1.1 Remote Sense

Pin 1 (+Remote Sense) and Pin 4 (-Remote Sense) are the pair of remote senses for single output modules, and main output V1 for the dual output module. Pin 9 (+Remote Sense V2) and Pin 10 (-Remote Sense V2) is the pair of remote sense for slave output V2 of the dual output module.

Connect the –RMT SENSE and +RMT SENSE to output 'V-' and 'V+' respectively at the point of load to compensate up to 500mV of voltage drop along the power cables, note that compensating too much voltage drop can cause overvoltage and latch the output. Leaving the remote sense floating will not cause the module to malfunction.





Rev.02.03.19\_#1.0 iVS Electrical Interface Page 14

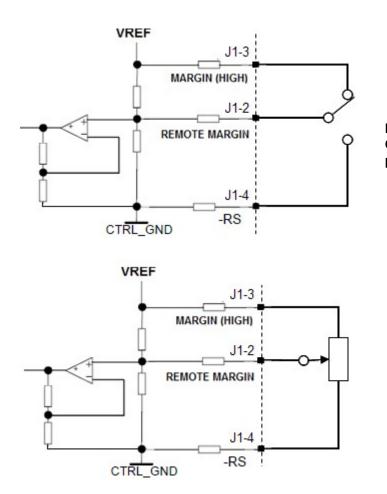
#### 2.1.2 REMOTE MARGIN/VPROG Pin 2 and MARGIN (HIGH) – Pin 3

Used to remotely adjust the output voltage regulation by +/- 4% - 6% from nominal setting.

Connect Remote Margin (Pin 2) to Margin High (Pin 3) to increase output voltage by 4%- 6% of the output setting. Connect Remote Margin (Pin 2) to –Remote Sense (Pin 4) to reduce the output voltage by 4% – 6%.

Note: The UVP and OVP threshold limits are reference to PMBus voltage setting and will not track with voltage adjustment of Remote Margin pins. Some modules have default UVP setting of 95% of nominal which is within the Remote Margin minimum of -6% of the nominal, adjust the UVP threshold to lower limit (e.g. <90%) to avoid hitting the UVP. The OVP limit is normally set to 115% of nominal which has enough margin from Remote Margin max +6% of nominal, the OVP limit can be set to 120% of nominal max if more margin is desired. The UVP and OVP can be adjusted using PMBus operation command.

Adjusting the voltage using the Trim-Pot of the modules has the same limitation as Vprog with respect to UVP and OVP setting.



Remote margining using Single Pole Center Off switch to achieve 3 possible voltage level.

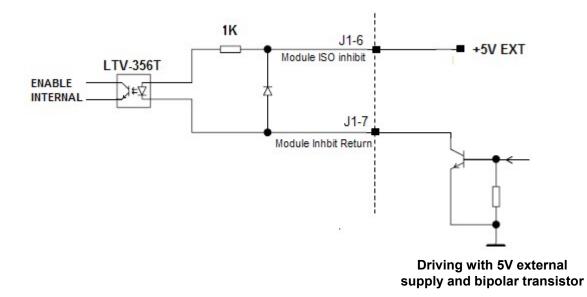
Remote margining using a potentiometer to get voltage adjustment range between 94% - 106% regulation of nominal rating.



Page 15

2.1.3 Module ISO Inhibit – Pins 6 and Module Inhibit Return - Pin 7

Isolated Inhibit input signals use to remotely enable/disable the module, apply 5V across the **Module ISO Inhibit and Module Inhibit Return** to disable the module. The 5Vstandby Housekeeping output can be used to drive Module Inhibit. When the module is turn OFF by the Inhibit pins, the PMBus MODULE OPERATION COMMAND alone CANNOT enable the module.

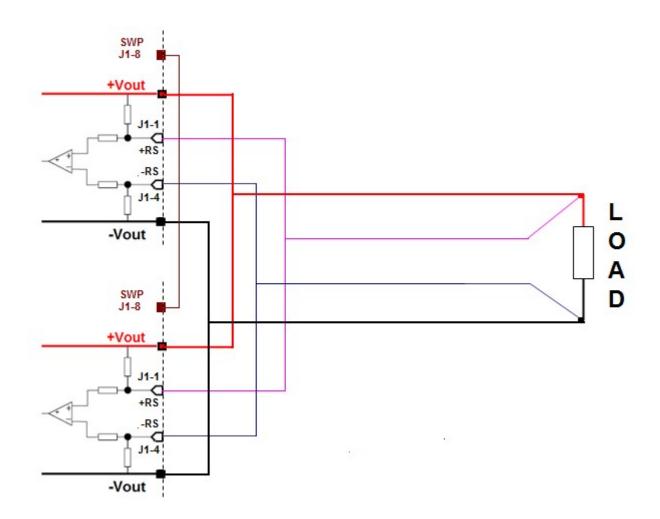


When a module is set to 'Module Enable Option 1' the output of the module is initially OFF, the PMBus MODULE OPERATION COMMAND alone CANNOT enable the module. The module can be enabled by applying 5V across Pin 6 and 7, the 5V standby Housekeeping output can be used to drive the pins. When the external voltage across Pin 6 and 7 is present to enable the module, the PMBus MODULE OPERATION command can be used to disable/enable the module.



### 2.1.4 Current Share (SWP) - Pin 8

Current Share Pin is an input/output signal of the module, when multiple modules are connected in parallel the Current Share Pins of each of the parallel modules must be connected together to achieve low error current sharing. Since, the output voltage of Current Share signal is proportional to the actual output current the pin can be used as output current monitor, the pin will have 6V nominal output at full rated load.



# 3. CAN/RS485 OPTION

For CAN/RS485 option, refer to application note

https://www.artesyn.com/power/power-supplies/product-docs/294/iVSmedical/trn\_can\_rs485\_interface\_adapte1321396157\_techref.pdf

### **WORLDWIDE OFFICES**

#### Americas

2900 S.Diablo Way Tempe, AZ 85282 USA +1 888 412 7832 Europe (UK) Waterfront Business Park Merry Hill, Dudley West Midlands, DY5 1LX United Kingdom

+44 (0) 1384 842 211

#### Asia (HK)

14/F, Lu Plaza 2 Wing Yip Street Kwun Tong, Kowloon Hong Kong +852 2176 3333



www.artesyn.com

For more information: www.artesyn.com/power For support: productsupport.ep@artesyn.com

While every precaution has been taken to ensure accuracy and completeness in this literature, Artesyn Embedded Technologies assumes no responsibility, and disclaims all liability for damages resulting from use of this information or for any errors or omissions. Artesyn Embedded Technologies, Artesyn and the Artesyn Embedded Technologies logo are trademarks and service marks of Artesyn Technologies, Inc. All other names and logos referred to are trade names, trademarks, or registered trademarks of their respective owners. © 2014 All rights reserved.